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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,194	08/30/2006	Steven T. Peake	GB04 0052 US1	5898
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NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131				
EXAMINER				
LEE, HSIEN MING				
ART UNIT		PAPER NUMBER		
2823				
NOTIFICATION DATE		DELIVERY MODE		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/591,194

Applicant(s)

PEAKE, STEVEN T.

Examiner

Hsien-ming Lee

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☒ Claim(s) 1-3,9 and 10 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date 20060830
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date ____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____

DETAILED ACTION

Claim Objections

1. Claims 1-3, 9 and 10 are objected to because of the following informalities:

In claim 1, at line 7, changing "the base" into – a base – suggested.

In claim 1, at lines 10, 15 and 16, changing "the trenches" into – the gate trenches – is suggested.

In claim 1, at line 12, changing "low doped region" into -- low-doped region – is suggested.

In claim 2, at line 2, inserting – region—after " drain" and "body" is suggested.

In claim 2, at line 2, inserting – gate – before "trenches" is suggested.

In claim 3, at line 2, inserting – insulated gate transistor-- before "structure" and at line 4, inserting – gate —before "trenches" are suggested.

In claim 9, at line 2, inserting – field effect – before "transistor –, at line 4, inserting – gate — before "trenches" and at line 6, changing "low doped region" into – low-doped region—are suggested.

In claim 10, at line 3, inserting –gate – before "trenches" is suggested.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5-8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The terms "lower-doped regions" and "higher-doped regions" in claim 5 (lines 3 and 4, claim 6 (lines 4 and 9) and claim 7 (lines 4 and 5) are relative terms which render the claim indefinite. The foregoing terms are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

In claims 8, (line 2) and 10 (lines 2-3), the term "the semiconductor" lacks antecedent basis.

In claim 10, at line 2, the limitation "etching the semiconductor away from the trenches" is not clear to the examiner. Does it mean – etching the substrate to form the gate trenches -- ?

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

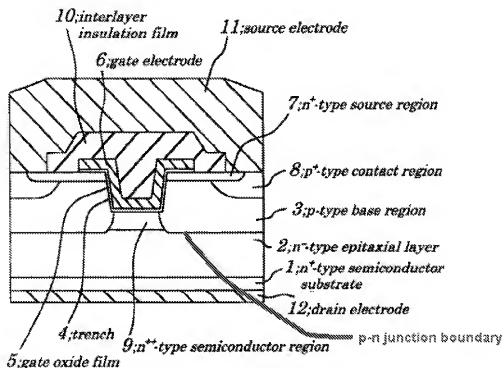
5. Claims 1-4, 8 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (US 6,160,288, submitted by applicant).

In re claim 1, Yamada, in Figs. 1-11 and corresponding text, A method of manufacturing an insulated gate field effect transistor; includes:

- providing a substrate 1 having a first major surface having a low-doped region 2 at the first major surface, the low-doped region 2 having a concentration of less than $5 \times 10^{14} \text{ cm}^{-3}$ (i.e. from 10^{13} to 10^{14} , col. 9, lines 20-21) at the first major surface;
- forming gate trenches 4 extending from the first major surface;
- forming trench insulator 5 on the base and sidewalls of the gate trenches 4;
- implanting dopants of a first conductivity type (i.e. n type) at the base of the trenches 4 (Fig.4);
- implanting a body implant of second conductivity type (i.e. p type) opposite to the first conductivity type (i.e. n type) in the low-doped regions between the trenches 4 to form a region 3;
- carrying out a diffusion step to form an insulated gate transistor structure in which the body implant diffuses towards the substrate 1 in the low-doped region 2 to form a p-n junction between a body region 3 doped to have the second conductivity type (i.e. p type) above a drain region (col. 8, line 51) doped to have the first conductivity type (i.e. n type), the p-n junction being deeper below the first major surface between the trenches than at the trenches; and
- forming source regions 7 at the first major surface adjacent to the trench 4.

In re claim 2, Yamada teaches that the p-n junction boundary between drain region and body region 3 is deeper between the gate trenches 4 than the depth of the gate trenches 4 (Fig.1).

Fig. 1



In re claim 3, Yamada teaches the diffusion step has an additionally doped region 9 of first conductivity type (i.e. n type) at the base of the gate trenches 4 having a doping density below $5 \times 10^{16} \text{ cm}^{-2}$ (i.e. from 10^{11} to 10^{13} cm^{-2} , col. 9, lines 42-45) but higher than in the drain region between the gate trenches 4.

In re claim 4, Yamada teaches that implants the body implant has dose of at most $5 \times 10^{13} \text{ cm}^{-2}$ (i.e. 10^{13} cm^{-2} , col. 9, lines 21-23).

In re claim 8, Yamada teaches that the substrate 1 is silicon because a thick oxide 16 is formed through oxidizing silicon; and the first conductivity type is n type.

In claim 9, the term "forming a convention insulated gate field effect transistor" renders indefinite as to what specific transistor is considered "conventional."

In re claim 11, Yamada teaches a trench FET formed by the method of claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Takei et al. (US 2005/0082640).

In re claim 9, the selection of the doping concentration is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. See M.P.E.P. 2144.05, III

In re claim 10, Yamada teaches etching the substrate 1 to form the gate trenches 4 but does not teach performing a moat etch.

Takei, however, in an analogous art of forming the gate trenches, teaches performing the moat etch (para [0136]) for forming the gate trenches.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to perform the moat etch, as taught by Takei et al., for forming the gate trenches of Yamada, since moat etch is an effective means for etching trenches.

Allowable Subject Matter

8. Claims 5-7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
9. The following is a statement of reasons for the indication of allowable subject matter:

None of the prior art of record, either taken alone or by combination, teaches or suggests forming a pattern laterally across the first major surface of the substrate the pattern doped to have [lower-doped] region of first conductivity type alternating with [higher-doped] region of first conductivity type.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Darwish et al. to US 7,033,876 teach a related art.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Monday through Friday (8:30 ~ 17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hsien-ming Lee/
Primary Examiner
Art Unit 2823

Sep. 27, 2008